

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	US 20040071193 A1	20040415	50	Path search method, channel estimation method and communication device	375/144	375/148
2	US 20010050950 A1	20011213	10	Received path timing detecting circuit at DS-CDMA system	375/150	
3	US 20010036221 A1	20011101	21	Path search circuit dividing a received signal into a plurality of FFT windows to reduce arithmetic operation processes for cross-correlation coefficients	375/147	
4	US 20010012316 A1	20010809	19	Rake receiver with low pass filter	375/148	375/149
5	US 6628698 B1	20030930	29	CDMA reception apparatus and power control method therefor	375/147	375/349; 455/134; 455/65
6	US 6590872 B1	20030708	16	Receiver with parallel correlator for acquisition of spread spectrum digital transmission	370/314	370/321; 370/337; 370/347; 370/442; 375/142; 375/147; 375/150; 375/219
7	US 6563859 B1	20030513	30	Receiver and receiving method in multi-carrier spread-spectrum communications	375/148	375/150; 375/152
8	US 6549527 B1	20030415	31	Radio receiver and despreader	370/342	342/373; 375/148; 455/562.1
9	US 6356542 B1	20020312	18	Reception path search method and searcher circuit of CDMA reception device	370/342	370/519; 375/147
10	US 6272167 B1	20010807	5	Spread spectrum communication system	375/144	370/335; 370/342; 375/147; 375/150; 375/347; 455/137
11	US 5999560 A	19991207	7	Rake reception method for a spread spectrum signal	375/148	375/347; 455/137
12	US 5982763 A	19991109	18	Reception timing detection circuit of CDMA receiver and detection method	370/342	370/335; 375/150; 375/343
13	US 5822364 A	19981013	19	Receiving apparatus for spectrum spread system	375/147	

	Inventor
1	Atarashi, Hiroyuki et al.
2	Sato, Toshifumi
3	Sato, Toshifumi
4	Maruyama, Yuichi
5	Oda, Toshiyuki
6	Shiue, Dong-Chang et al.
7	Oishi, Yasuyuki et al.
8	Tsutsui, Masafumi et al.
9	Hayata, Toshihiro
10	Ono, Shigeru
11	Ono, Shigeru
12	Sato, Toshifumi
13	Yamada, Daisuke et al.

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	US 20030169838 A1	20030911	21	EMI reduction using tunable delay lines	375/376	
2	US 20030118142 A1	20030626	22	Scalable high-speed precision frequency and phase synthesis	375/376	
3	US 20030091138 A1	20030515	19	Data clock regenerating apparatus	375/376	
4	US 20020154723 A1	20021024	53	Oversampling clock recovery having a high follow-up character using a few clock signals	375/376	
5	US 20020034274 A1	20020321	15	Phase detector and phase locked loop circuit	375/376	375/340
6	US 20010006544 A1	20010705	25	Frequency synthesizer	375/376	327/156
7	US 6636575 B1	20031021	14	Cascading PLL units for achieving rapid synchronization between digital communications systems	375/376	327/149; 327/150; 331/17; 341/126; 341/128; 341/129; 341/143; 341/144; 341/146; 341/61; 375/241; 375/242; 375/282; 375/354; 375/371; 375/373; 375/374; 375/375; 375/377
8	US 6564039 B1	20030513	12	Frequency generation circuit and method of operating a transceiver	455/76	331/34; 375/376; 455/265; 455/78
9	US 6509776 B2	20030121	17	DLL circuit, semiconductor device using the same and delay control method	327/277	327/158; 327/161; 327/284; 331/DIG.2

	Inventor	Image Doc. Displayed
1	Greenstreet, Mark R. et al.	US 20030169838
2	Xiu, Liming et al.	US 20030118142
3	Tagami, Hitoyuki	US 20030091138
4	Nakamura, Satoshi	US 20020154723
5	Yabe, Tomoaki	US 20020034274
6	Kawasaki, Somei et al.	US 20010006544
7	Ott, Stefan	US 6636575
8	Meador, Richard B. et al.	US 6564039
9	Kobayashi, Shotaro et al.	US 6509776

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
10	US 6211741 B1	20010403	7	Clock and data recovery PLL based on parallel architecture	331/11	327/147; 331/1A; 331/12; 375/376
11	US 6178216 B1	20010123	21	Digital phase locked loop circuit and method therefor	375/376	327/147
12	US 6148052 A	20001114	15	Digital phase detector with ring oscillator capture and inverter delay calibration	375/375	327/159; 331/25; 331/57; 375/376
13	US 6125158 A	20000926	16	Phase locked loop and multi-stage phase comparator	375/376	327/156; 327/158; 327/159; 327/236; 327/244; 331/10; 331/11; 331/25; 375/327; 375/371; 375/373; 375/374; 375/375
14	US 6046643 A	20000404	4	Radio-frequency signal generator	331/1A	327/107; 331/25; 375/376
15	US 5648964 A	19970715	28	Master-slave multiplex communication system and PLL circuit applied to the system	370/228	370/517; 375/357; 375/376
16	US 5095233 A	19920310	25	Digital delay line with inverter tap resolution	327/149	327/150; 327/277; 331/DIG.2 ;
17	US 5079519 A	19920107	25	Digital phase lock loop for a gate array	331/1A	327/231; 327/43; 331/17; 375/376
18	US 4400667 A	19830823	9	Phase tolerant bit synchronizer for digital signals	331/1A	331/17; 331/34; 331/DIG.2 ;
19	US 4301417 A	19811117	15	Quadriphase differential demodulator	329/310	375/331; 375/357; 375/376

	Inventor	Image Doc. Displayed
10	Dalmia, Kamal	US 6211741
11	Lee, Ig-yong	US 6178216
12	Bogdan, Wladyslaw	US 6148052
13	Carson, Dave et al.	US 6125158
14	Kranz, Christian	US 6046643
15	Inagaki, Yoshio et al.	US 5648964
16	Ashby, Laurin et al.	US 5095233
17	Ashby, Laurin et al.	US 5079519
18	Belkin, Martin	US 4400667
19	Jansen, Augustinus M. et al.	US 4301417

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
20	US 4019153 A	19770419	24	Digital phase-locked loop filter	331/1A	327/12; 327/231; 327/5; 329/311; 331/17; 331/25; 375/376

	Inventor	Image Doc. Displayed
20	Cox, Jr., Duncan B. et al.	US 4019153

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1	BRS	L1	21760	(delay\$3 near3 clock\$) or (phase\$ near3 shift\$3 near2 clock\$3) or (phase\$ near3 invert\$3 near3 clock)	USPA T	2004/01/12 13:58	
2	BRS	L2	2145	375/238.ccls. or 341/53.ccls. or 329/316.ccls. or 332/109.ccls. or 375/238.ccls. or 327/172.ccls. or 327/31.ccls. or 327/26.ccls. or 370/205.ccls.	USPA T	2004/01/12 13:54	
3	BRS	L3	182	1 and 2	USPA T	2004/01/12 13:55	
4	BRS	L4	53	1 and 2 and ((pwm) or (pulse near2 width near2 modulats3))	USPA T	2004/01/12 13:56	
5	BRS	L5	26366	((pwm) or (pulse near2 width near2 modulats3))	USPA T	2004/01/12 13:56	
6	BRS	L6	53	13 and 15	USPA T	2004/01/12 13:57	
7	BRS	L7	153	((delay\$3 near3 clock\$) or (phase\$ near3 shift\$3 near2 clock\$3) or (phase\$ near3 invert\$3 near3 clock\$)) same ((pwm) or (pulse\$ near2 width near2 modulats3))	USPA T	2004/01/12 14:15	
8	BRS	L8	15196	((delay\$3 near3 clock\$) or (phase\$ near3 shift\$3 near2 clock\$3) or (phase\$ near3 invert\$3 near3 clock\$)) same ((pwm) or (pulse\$ near2 width near2 modulats3)) same3 (rising near5 falling)	USPA T	2004/01/12 14:01	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
9	BRS	L9	6	((delay\$3 near3 clock\$) or (phase\$ near3 shift\$3 near2 clock\$3) or (phase\$ near3 invert\$3 near3 clock\$)) same ((pwm) or (pulse\$ near2 width near2 modulat\$3)) same (rising near5 falling))	USPA T	2004/01/12 14:16	
10	BRS	L10	144	((delay\$3 near3 clock\$) or (phase\$ near3 shift\$3 near2 clock\$3) or (phase\$ near3 invert\$3 near3 clock\$)) and ((pwm) or (pulse\$ near2 width near2 modulat\$3)) and (rising near5 falling))	USPA T	2004/01/12 14:18	
11	BRS	L11	11	l10 and l2	USPA T	2004/01/12 14:18	

	U	1	Document ID	Issue Date	Pages	Title	Current OR
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6512534 B2	20030128	21	Clock control apparatus and method and image forming apparatus using clock control apparatus	347/249
2	<input type="checkbox"/>	<input type="checkbox"/>	US 5583552 A	19961210	24	Optimum phase determination based on the detected jet current	347/80
3	<input type="checkbox"/>	<input type="checkbox"/>	US 5535187 A	19960709	35	High capacity run-length-limited coding system employing asymmetric and even-spaced codes	369/59.2
4	<input type="checkbox"/>	<input type="checkbox"/>	US 5450111 A	19950912	25	Ink jet recording apparatus having drop-registration adjusting system	347/78
5	<input type="checkbox"/>	<input type="checkbox"/>	US 5191518 A	19930302	18	Plural inverter control arrangement	363/71
6	<input type="checkbox"/>	<input type="checkbox"/>	US 4882120 A	19891121	17	DC content control for an inverter	363/98

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6	US 4882120	<input type="checkbox"/>

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1	<input type="checkbox"/>	<input type="checkbox"/>	US 6658583 B1	20031202	18	PWM control circuit, microcomputer and electronic equipment	713/500
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6390579 B1	20020521	19	Pulse width modulator using delay-line technology with automatic calibration of delays to desired operating frequency	347/9
3	<input type="checkbox"/>	<input type="checkbox"/>	US 5963106 A	19991005	20	Double-sided pulse width modulator	332/109
4	<input type="checkbox"/>	<input type="checkbox"/>	US 5880644 A	19990309	9	N-bit pulse width modulated signal generator	332/109
5	<input type="checkbox"/>	<input type="checkbox"/>	US 5615228 A	19970325	41	Apparatus and method to decode a pulse width modulated serial data stream	375/238
6	<input type="checkbox"/>	<input type="checkbox"/>	US 5548286 A	19960820	61	Analogue and digital convertors using pulse edge modulators with non-linearity error correction	341/126
7	<input type="checkbox"/>	<input type="checkbox"/>	US 5438303 A	19950801	54	Pulse with modulation apparatus with plural independably controllable variable delay devices	332/109
8	<input type="checkbox"/>	<input type="checkbox"/>	US 5428321 A	19950627	44	Pulse width modulator having controlled delay circuit	332/109
9	<input type="checkbox"/>	<input type="checkbox"/>	US 5304855 A	19940419	14	Bi-level pulse accumulator	327/31
10	<input type="checkbox"/>	<input type="checkbox"/>	US 4658225 A	19870414	33	Amplitude insensitive delay lines in a transversal filter	333/166
11	<input type="checkbox"/>	<input type="checkbox"/>	US 4603301 A	19860729	32	Amplitude insensitive delay lines in a frequency modulated signal detector	329/319

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